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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/815,709	04/02/2004	Naoki Kuroda	60188-763	9729
7590 08/08/2005 McDermott, Will & Emery 600 13th Street, N. W. Washington, DC 20005-3096			EXAMINER TRAN, MICHAEL THANH	
			ART UNIT 2827	PAPER NUMBER

DATE MAILED: 08/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/815,709	KURODA ET AL.	
	Examiner	Art Unit	
	Michael t. Tran	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on April 2, 2004 through December 30, 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 15-24 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 15 and 20 is/are rejected.
- 7) ☒ Claim(s) 16-19 and 21-24 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☒ Certified copies of the priority documents have been received in Application No. 10/233,486.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 040204&123004.

- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

[Signature]
MICHAEL T. TRAN
PRIMARY EXAMINER

DETAILED ACTION

1. In response to the Communications dated April 02, 2004 through December 30, 2004, claims 15-24 are active in this application as a result of the cancellation of claims 1-14 and 25-29.

Foreign Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a) (d), which papers have been placed of record in the file.

Information Disclosure Statement

3. The information disclosure statements filed April 02, 2004 and December 30, 2004 have been considered.

Claim Objections

4. Claims 16-19 and 21-24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections – 35 U.S.C. § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

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A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in-

(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or

(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

6. Claim 15 is rejected under 35 U.S.C 102(b) as being anticipated by Chang et al. [U.S. Patent #6,111,796].

With respect to claim 15, Chang et al. disclose, in column 6, lines 40-65, a semiconductor memory device, comprising: a first main amplifier [30] activated in response to an active first enable signal [49], for amplifying data read from a first memory cell; a first tri-state buffer [within element 44] for driving an output node of the first tri-state buffer according to the data amplified by the first main amplifier when the first enable signal is active, and rendering the output node in a high impedance state when the first enable signal is inactive; and a first latch circuit [within output stage of element 44] for latching and outputting data of the output node of the first tri-state buffer to the outside.

7. Claim 20 is rejected under 35 U.S.C 102(e) as being anticipated by Gray [U.S. Patent #6,484,271].

With respect to claim 20, Gray discloses, in figure 1, a semiconductor memory device, comprising: an output buffer [44 and 54] for outputting data read from a memory cell to an output terminal, wherein the output buffer includes a first buffer [44] for driving the output terminal [q] according to the data read from the memory cell, and a second buffer [54] having an active state and an inactive state, for driving the output terminal according to the read data in the active state.

Allowable Subject Matter

8. The following is an Examiner's statement of reasons for the indication of allowable subject matter: the prior art of records does not show (in addition to the other elements in the claim) the following:

- A switch connected between the output node of the tri-state buffer and the second latch circuit, for connecting the output node of the tri-state buffer to the second latch circuit in a test mode, and disconnecting the output node of the tri-state buffer from the second latch circuit in a normal mode.
- A second tri-state buffer for driving an output node of the second tri-state buffer according to the data amplified by the second main amplifier when the second enable signal is active, and rendering the output node in a high impedance state when the second enable signal is inactive; a second latch circuit for latching and output data of the output node of the second tri-state buffer to the outside.
- The second buffer is activated and inactivated according to a bit width of the data read from the memory cell.

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- A detector for detecting an operating frequency of the semiconductor memory device, wherein the second buffer is activated and inactivated according to the operating frequency detected by the detector.

Conclusion

9. When responding to the Office action, Applicants are advised to provide the Examiner with line and page numbers of the application and/or references cited to assist the Examiner in the prosecution of this case.

10. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Michael T. Tran whose telephone number is (571) 272-1795. The Examiner can normally be reached on Monday-Thursday from 7:30-6:00 P.M.

11. Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (571) 272-1650.



Michael T. Tran
Art Unit 2827
August 3, 2005

MICHAEL TRAN
PRIMARY EXAMINER